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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,373	07/01/2003	Wee-Kuan Gan	4413-0113P	1209

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EXAMINER	
RUTZ, JARED IAN	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 12/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,373	GAN ET AL.	
	Examiner	Art Unit	
	Jared I. Rutz	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-5 as amended on 10/24/2005 are pending in the instant application. Of these, there are 1 independent and 4 dependent claims. Applicant's arguments filed 10/24/2005 have been carefully and fully considered, however they are not persuasive. Accordingly, this action is made **FINAL**.

Drawings

2. The drawings were received on 10/24/2005. These drawings are not fully acceptable. In figure 7 item 490 is not clearly connected to the flowchart. It is not clear if the no branch from item 480 goes to item 490 or if the no branch goes around item 490. The same is true of item 570 of figure 8. Item 480 does not indicate a decision. Examiner recommends removing "then stop the reading" from item 480 and placing it in a separate item which is reached from a yes decision on item 480. Figure 8 item 550 is not a step as it lacks a verb.

Specification

3. The amendment to the specification filed 10/24/2005 is accepted by the examiner and is sufficient to overcome the objections to the specification. Accordingly the objection to the specification is withdrawn.

Claim Rejections - 35 USC § 112

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. **Claim 1** is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for writing to a block that already contains data does not reasonably provide enablement for writing to a block that does not already contain data. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make or use the invention commensurate in scope with these claims. The steps of writing to a sector of one of the blocks are not limited to the case in which there has already been data written to the block to which a write is desired. In the case of a first write to a logical block, there is no plurality of pages prior to the one page in to which the sector to be written that contain data that can be read out. Accordingly, the claim is not limited to embodiments for which the disclosure is enabling.

6. The amendment to **claim 4** is sufficient to overcome the rejection under 35 USC 112 first paragraph. Accordingly, said rejection has been withdrawn.

7. The amendment to **claim 3** is sufficient to overcome the rejection under 35 USC 112 second paragraph. Accordingly, said rejection is withdrawn.

8. The amendment to **claim 4** is sufficient to overcome the rejection under 35 USC 112 second paragraph. Accordingly, said rejection has been withdrawn.

Claim Rejections - 35 USC § 103

9. **Claims 1-5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hieberger et al (US 5341,489) in view of Pua et al (US 2002/0147882).

10. **Claim 1** is taught by Heiberger as:

a. An interleaving management method for upgrading a data processing speed of a flash memory, comprising a plurality of flash memory cells. See column 2 lines 59-65.

b. Wherein each of said flash memory cells comprises a plurality of blocks for reading and writing data and a plurality of pages in each said blocks. Typically in flash memory, a block is the smallest set of erasable memory, and a page is the smallest set of data that is written in a single operation. See column 5 lines 58-63 which states that on some devices erasure is performed on a substantial portion of a flash memory, which shows that there are multiple blocks. See also figure 7 and column 7 lines 61-66, which shows multiple bytes in each block. In the given illustration of the invention there is only one block for each memory device, however it is shown (column 5 lines 58-63) that the invention can also be used with memory devices having multiple erasure blocks.

c. Continuously writing data into said plurality of flash memory cells, wherein when writing two or more sets of sectors into said plurality of flash memory cells, write a first sector into a first flash memory cell, and while the process of writing said first sector into said first flash memory cell is ongoing, a second flash memory cell is enabled so that a second sector can be written into said second

flash memory cell. See column 3 lines 1-4, which state that data is latched in sequence and programmed in tandem. Figure 8 illustrates this operation. The first page is latched into the first memory device, and while it is being written, data is latched into a second memory device. Latching data into the second memory device enables the second memory device to record the data.

11. Heiberger does not disclose the use of the memory cells in a mother and child structure.

12. **Claim 1** is taught by Pua as:

d. Wherein the step of writing one of the sectors into one page of one of the blocks includes: defining the one of the blocks as a mother block. The mother block is defined as the block corresponding to the logical address received from the host in paragraph 0118.

e. Selecting a backup block as a child block. See paragraph 0121.

f. Assigning the child block a logical address same as a logical address of the mother block. See paragraph 0033, which shows that the mother block and the child block have the same logical address.

g. Reading out a plurality of pages prior to the one page into which the sector to be written from the mother block and writing the plurality of pages prior to the one page into the child block. See paragraph 0123.

h. And writing the one of the sectors into the one page. See paragraph 0124, which discusses step 608 of figure 6, in which the data is written to the child block.

i. Heiberger and Pua are analogous art because they are from the same field of endeavor, namely the design of portable flash memory based storage devices.

j. At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the overwrite method disclosed by Pua in a memory card using the interleaving structure of Heiberger. The motivation for doing so would be to extend the life of the flash memory cells (see paragraph 0029 of Pua). Additionally, a stated limitation of Heiberger is that deleting a set of data corresponding to a single image that is spread over multiple blocks would require erasing all the blocks. The use of Pua's copy technique would allow the data in the blocks to be deleted to be easily saved within the memory device.

13. Therefore it would have been obvious to combine Pua with Heiberger for the benefits of extending the life of the flash memory and easily deleting an image without deleting other images stored in the same blocks to obtain the invention as specified in claim 3.

14. **Claim 2** is taught by Heiberger as:

k. Wherein said a plurality of flash memory cells for continuously writing data are arranged in an interleave structure. See figure 1, which illustrates the arrangement of the memory cells for the interleaving method of the invention.

15. **Claim 3** is taught by Pua as:

l. Wherein the step of writing the one of the sectors into the one page includes: when the one of the sectors is not a last set of the data, writing a next

sector of the data into a page of the child block immediately following the one page. See paragraphs 122-126, which show that if there is more data to be written, it is written to the child block.

m. Erasing the mother block after writing a last sector of the data into the child block. See paragraph 0128.

16. **Claim 5** is taught by Heiberger as:

n. Wherein said interleaving management method for managing data processing of a plurality of flash memory cells is suitably applied in a hosting device, wherein said hosting device includes at least one of, a portable ROM, a card reader in USB1.1 series, acard reader in USB2.0 series, and an IDE/PCMCIA interface. See column 1 lines 6-9, which show that the interleaving system is used in a flash memory card, and column 3 lines 65-86 which show that the card is removable.

17. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Heiberger in view of Pua further in view of Applicant's admitted prior art.

o. Heiberger in view of Pua discloses a memory interleaving method as shown with respect to claims 1 and 2 above. Heiberger in view of Pua does not disclose expressly the use of memory cells utilizing the copy back command.

p. The copy back command is identified as being known in the art in paragraph 0013 of the applicant's specification. As stated in the application, the use of memory cells incorporating a copy back command is beneficial as it allows

data to be read from and written to the flash memory fewer times, which allows more efficient use of the memory.

q. As the invention disclosed by Heiberger in view of Pua deals with reading from and writing to flash memory, it would be obvious to one skilled in the art to use flash memory that implements the copy back command to implement the memory interleaving method and mother/child structure disclosed by Heiberger in view of Pua. This would allow a more efficient use of the memory cells.

r. According to page 12 lines 19-20 of the applicant's specification, the use of two memory cells is used only as an example to illustrate the operation of the disclosed invention. The specifications of the memory cells chosen in a given implementation would be specific to the to the design needs of the implementation.

18. Therefore, it would have been obvious to combine the Applicant's admitted prior art with the memory interleaving method and mother/child structure of Heiberger in view of Pua for the benefit of an efficient implementation of Heiberger in view of Pua's interleaving method and mother/child structure to obtain the invention as specified in claim 4.

Response to Arguments

19. Applicant's arguments filed 10/24/2005 have been fully considered but they are not persuasive.

20. The objection to the specification has been withdrawn as stated supra.

21. The objection to the drawings has not been withdrawn, for the reasons stated supra.

22. The previous rejections under 35 USC 112 first paragraph and second paragraph have been withdrawn as stated supra. However a new rejection to claim 1 as stated supra necessitated by the amendment to claim 1 has been presented supra.

23. With respect to the first full paragraph of page 9, the rejection under 102(b) has been overcome by amendment. The new grounds of rejection of claim 1 under 35 USC 103, relying on the same references used in the previous Office Action, has been necessitated by the amendment to claim 1 and is presented supra.

24. In the second paragraph of page 9, Applicant argues that Pua merely discloses that the child physical block number is filled into the mother block's logical block address, and that Pua fails to teach "reading out a plurality of pages prior to the one page into which the sector to be written from the mother block and writing the plurality of pages prior to the one page into the child block; and writing the one of the sectors into the one page" as recited in claim 1. The examiner respectfully disagrees, and directs Applicant to the rejection of claim 1 under 35 USC 103 supra.

Conclusion

25. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jared I Rutz
Examiner
Art Unit 2187

jir

DONALD SPARKS
SUPERVISORY PATENT EXAMINER